

## CLAIMS

What is claimed is:

1. An integrated circuit package comprising:

    a substrate having first and second surfaces and a plurality of conductive traces therebetween;

    a semiconductor die flip-chip mounted to said first surface of said substrate and electrically connected to ones of said conductive traces;

    an intermetallic heat spreader fixed to a back side of said semiconductor die; and

    a plurality of contact balls disposed on said second surface of said substrate, in the form of a ball grid array, ones of said contact balls of said ball grid array being electrically connected with ones of said conductive traces.

2. The integrated circuit package according to claim 1, wherein said semiconductor die is flip-chip mounted to said first surface of said substrate and electrically connected to ones of said conductive traces via a plurality of solder ball connectors.

3. The integrated circuit package according to claim 2, further comprising an underfill material surrounding said solder ball connectors.

4. The integrated circuit package according to claim 1, wherein said solder ball connectors are comprised of eutectic solder.

5. The integrated circuit package according to claim 1, wherein said intermetallic heat spreader is fixed to said back side of said semiconductor die by a thermally conductive adhesive.

6. The integrated circuit package according to claim 1, wherein said intermetallic heat spreader is fixed to said back side of said semiconductor die by a thermally conductive epoxy.

7. The integrated circuit package according to claim 1, wherein said intermetallic heat spreader comprises a first portion fixed to said back side of said semiconductor die and a plurality of sidewalls in contact with said substrate.

8. The integrated circuit package according to claim 7, wherein said sidewalls are fixed to said substrate.

9. The integrated circuit package according to claim 1, wherein said heat spreader is fixed to a plurality of intermediate sidewalls at a plurality of sites, each of said intermediate sidewalls being fixed to said substrate.

10. The integrated circuit package according to claim 9, wherein said intermediate sidewalls comprise an intermetallic material.

11. The integrated circuit package according to claim 1, wherein said intermetallic compound comprises an intermetallic compound having a coefficient of thermal expansion of from about 18 ppm/ $^{\circ}$ C to about 26 ppm/ $^{\circ}$ C.

12. The integrated circuit package according to claim 1, wherein said intermetallic compound comprises an intermetallic compound having a coefficient of thermal expansion of about 22 ppm/ $^{\circ}$ C.

13. The integrated circuit package according to claim 1, wherein intermetallic compound comprises CuAl<sub>3</sub>.

14. The integrated circuit package according to claim 1, wherein said intermetallic compound has a modulus of elasticity of at least the modulus of elasticity of the semiconductor die.

15. The integrated circuit package according to claim 1, wherein said intermetallic compound comprises NiAl.

16. An integrated circuit package comprising:  
a substrate having first and second surfaces and a plurality of conductive traces therebetween;  
a semiconductor die flip-chip mounted to said first surface of said substrate and electrically connected to ones of said conductive traces;

a heat spreader having a coefficient of thermal expansion in the range of about 18 ppm/ $^{\circ}$ C to about 26 ppm/ $^{\circ}$ C, fixed to a back side of said semiconductor die; and

a plurality of contact balls disposed on said second surface of said substrate, in the form of a ball grid array, ones of said contact balls of said ball grid array being electrically connected with ones of said conductive traces.

17. The integrated circuit package according to claim 16, wherein the heat spreader has a coefficient of thermal expansion of about 22 ppm/ $^{\circ}$ C.

18. The integrated circuit package according to claim 16, wherein said intermetallic compound has a modulus of elasticity of at least the modulus of elasticity of the semiconductor die.